Keith Gerhardt 978.732.7069 keith@keithgerhardt.com

Objectives

Lead/Senior Engineer level position in a research and development organization.

Strengths

Extensive experience in bringing products to market. Hands on, in-depth work with many networking protocols. Hardware experience covers system design, FPGA (Xilinx/Altera), Verilog, VHDL and simulation (Modelsim/Synopsis), schematic capture and board layout. All programs have COTS exposure.

Experience in C/C++, Java language and various assembly languages. Use of a variety of tools, debuggers, in-circuit emulators, network analyzers and logic analyzers, RTOS, VxWorks, Eclipse IDE, SVN, git. Excellent problem solving skills and quick learning. Unix, Linux and Windows operating systems experience.

Experienced project leadership, delivering on time and under budget. Providing leadership and mentoring to multidiscipline teams both in multiple states and internationally.

Experience

Heme Photonics

Worked with a colleague and a UMass physician to develop a system to remove carbon monoxide from blood stream with light (laser/LED) to treat patients affected with CO poisoning. Provided an engineering approach to the team's knowledge base.

Laser Light Engines

Developing control and monitoring solutions for laser systems. HW Design and proto debug of micro controller based embedded systems and PC based management supervisor with Altera FPGA. Ported RTOS to micro controller, developed application and test routines in C. Developed Debian Linux based system for control, monitoring and logging of slaves over a network, developed device drivers for FPGAs. Very small team, multiple roles.

Sycamore Networks

Retarget FPGA from Xilinx Virtex 2 Pro to Virtex 5 to eliminate manufacturing and support issues. Design function was to connect a part with a SPI4.2 interface to a part with a XAUI interface. Design had many cores (50+) and timing constraints that needed translation. Managed project schedule and simulation resource as well as performing a majority of the translation and regression testing work.

Evaluated system needs for next generation Metro Ethernet Forum transport switch through development of a Marketing Requirements Document and Product Architecture Specification. Includes definition of control plane, selection of vendor and in-house components and cost modeling. COTS and component solutions studied.

Design 1 and 10 Gigabit Ethernet interface cards for new chassis. Worked with Marketing to define system needs from requirements documents, developed project schedule, wrote board specifications, selected components to meet needs and schedule. Performed tasks from design through bring up and release to manufacturing.

Mercury Computer

Contractor – Complete hardware design, direct board layout, write VHDL code for CPLD/FPGAs, manage manufacturing issues with prototype builds of board for a base station chassis. Managed project made up of an international team. Design for COTS.

Ciena Corp

Member of Tech Staff - Development of 10 Gigabit card for Ciena CN 4350 chassis. Directed 8-plus member team through individual contribution, task assignment, problem resolution and status meetings. Card had both a LAN 10 Gb Ethernet and a WAN OTU-2 /G.709 interfaces. Based on AMCC framer and Marvell network processor/switch fabric with Xilinx Virtex 2 Pro FPGA utilizing XAUI and SPI4.2 interfaces to buffer traffic to match clock rates between disparate interfaces. Coding performed in VHDL, interfaced with third-party Verilog components. Performed selection and design for discrete clock components used in conjunction with on-board PLLs. Coded and reviewed low level software in C under an embedded Linux OS that interfaced to components.

Performed part selection, schematic capture, and initial placement. Generated routing requirements, worked with internal and contract PCB designers and mechanical engineers. Worked BOMs through Agile with purchasing and contract manufacturer to produce multiple builds of prototype units. Tested, configured and debugged units during software integration. Debugged FPGA design in system, making changes and compiling with Xilinx ISE.

Coriolis Networks, Boxborough MA

Project Lead / Senior Member of Tech Staff - Lead project teams designing switch modules for 2 Metro Optics hubs. Architected products to provide a lower operating cost, higher margin services by regional and small market TELCOs. Hubs interfaced to metro OC-48 SONET rings to provide managed bandwidth for T1, DS1, T3, OC-12 and 10/100/1000 Ethernet connections. Hubs were designed to be NEBS Level 3 compliant operating at a CO. Performed device selection, schematic capture and simulation. Used high density CPLDs and FPGAs to meet cost and time to market targets. Developed schedules and documented designs. Worked with software director to task software engineers during each phase, personally coding sections to speed development. Tasked software engineers to develop BSP and diagnostics. Wrote diagnostics and low level firmware modules. Used PCB tool (Allegro) to place components and route critical etch. Designed modules for FCC compliance, working with compliance engineers during testing phase. Performed DVT and signal quality analysis on all interfaces. Generated test documents for technicians to efficiently debug boards on their own.

MMC Networks, Chelmsford MA

Member of Tech Staff - Designed 24 Port 10/100 Ethernet switch with Gigabit uplink using MMC chips. Product used as reference design for customers developing systems with MMC chips. Responsibilities included selecting components, schematic capture, coding FPGA, contract layout, work with manufacturer, verifying and debugging design, software integration on platform, developing manufacturing test scripts, programmed network processors.

THiiNLine Business Unit, Data General Corporation

Staff Engineer – Lead design of a wireless access point product. Designed X86 based board performing part selection and schematic capture, worked with external layout and manufacturing groups to build board. Assured that design met FCC Class B.

Lead team of software engineers at DG Research Triangle Park, NC facility implementing a flash memory based embedded Linux operating system and applications for product. Developed software release schedule and tasked software engineers to meet schedules. Incorporated flash file system for parameter files.

Digital Equipment Corporation, Littleton, MA, Networks Engineering

Team Leader/Consulting Engineer on several networking projects. Highly visible projects that were delivered on time, producing over 50M in revenue. Lead Architect for DEChub 900. Held several positions in different groups over time in the company.

Lead engineers in developing switched Ethernet and Token Ring products. Implemented FPGA using VHDL and Synopsis tool set. Designed hardware module, worked physical layout plan, prototype build. Verified and debugged with logic analyzers and C code scripts. Completed transition to manufacturing.

Education

MSEE/Computer Engineering, *Worcester Polytechnic Institute*, Worcester, MA.

BSEE, *Worcester Polytechnic Institute*, Worcester, MA.